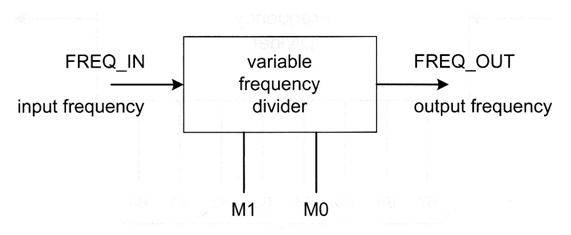
**Activity 3: (Problem 14A.6)**

* Variable frequency divider
* Design a variable frequency divider using AHDL. The frequency divider should divide the input frequency by one of four different factors. The divide-by-factor is controlled by two mode controls, as described by the following function table. The mode controls are used to change the modulus of the counter used for the frequency division. The output waveform will be high for two clock cycles starting at state zero. Hint: Define buried combinational circuit nodes (in the VARIABLE section) that can define (in the Logic section with Boolean expressions) the four different conditions that can exist when the counter should be recycled. Compile and simulate your results. Submit both your AHDL and waveform file.

|  |  |  |
| --- | --- | --- |
| M1 | M0 | Divide by: |
| 0 | 0 | 5 |
| 0 | 1 | 10 |
| 1 | 0 | 12 |
| 1 | 1 | 15 |



**Read Unit 15 in your lab manual.**

**Activity 4: (Problem 15.6)**

* Mod-31 LFSR counter
* Design a mod-31 LFSR counter using AHDL. The counter should have two synchronous controls, an active-low reset (resetn), and an active-high count enable (enable). Compile and simulate your results. Submit both your AHDL and waveform file.